ABSTRACT OF THE DISCLOSURE

A method for testing a memory cell array of a semiconductor memory device in a parallel bit test mode includes selecting first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad, and then selecting second data from another of the plurality of memory regions for output via the input/output pad. The first and second data can be selected from memory regions sharing a row select or a column select control line. Alternatively, one of the first and second data can be selected from memory regions sharing a row select control line, and the other can be selected from memory regions sharing a column select control line. Therefore, a parallel bit test can be performed using fewer input/output pads, and a larger number of semiconductor memory devices can simultaneously be tested. Related circuits are also discussed.